Figure 1a

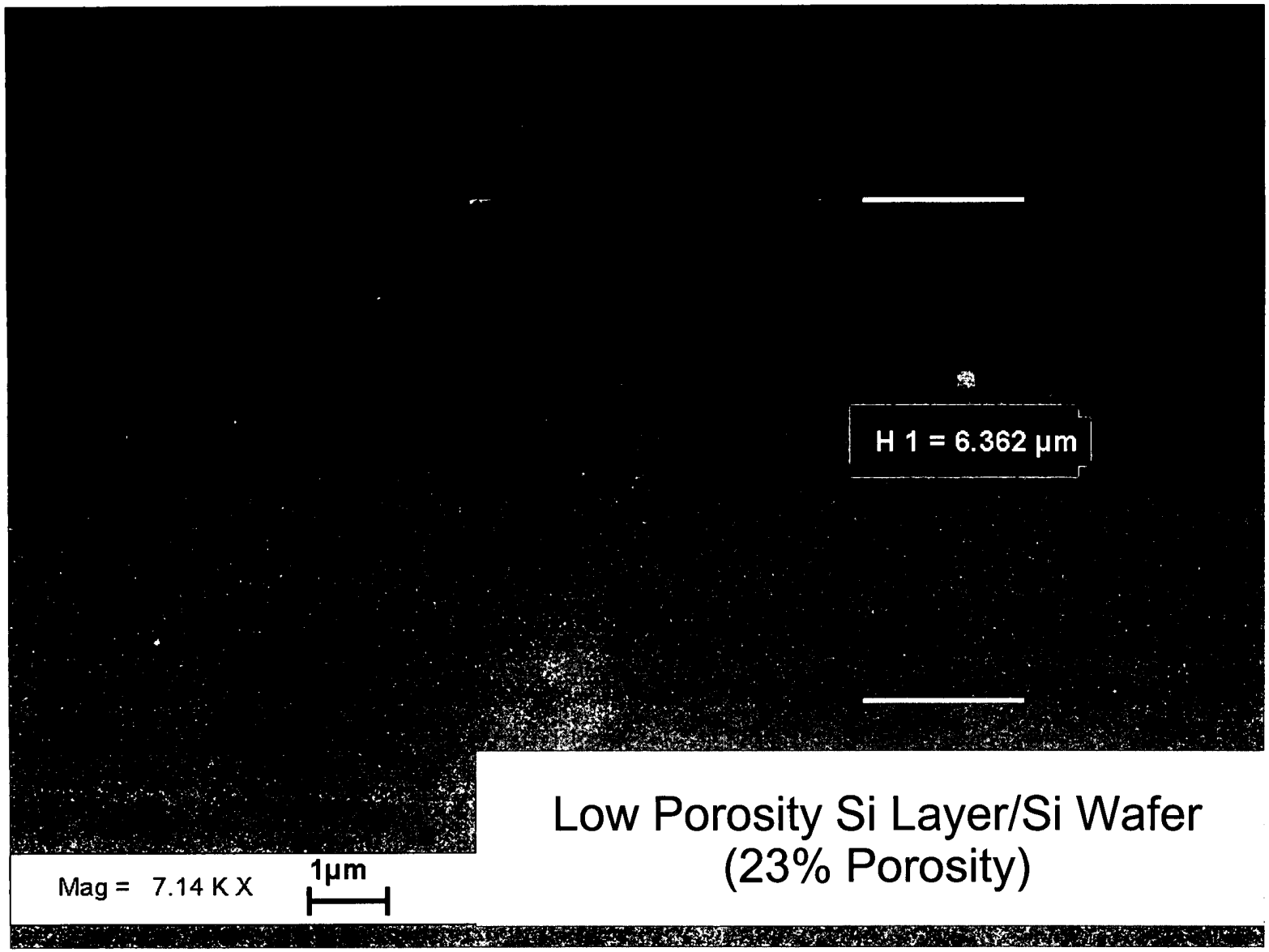

H 1 = 6.362 µm
Mag = 7.14 K X
1µm
Low Porosity Si Layer/Si Wafer
(23% Porosity)

Figure 1b

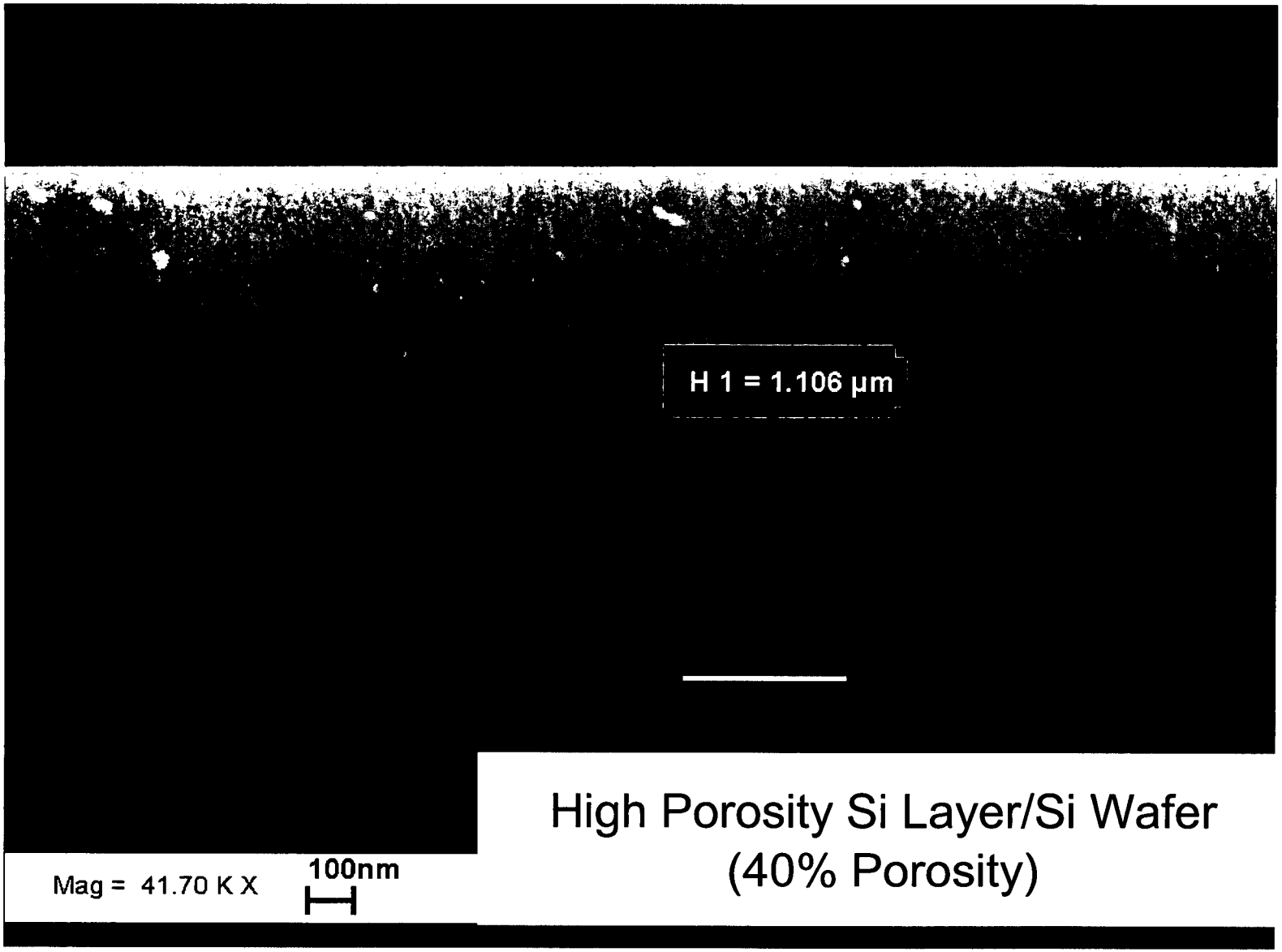

H 1 = 1.106 µm
Mag = 41.70 K X
100nm
High Porosity Si Layer/Si Wafer
(40% Porosity)

Figure 1c

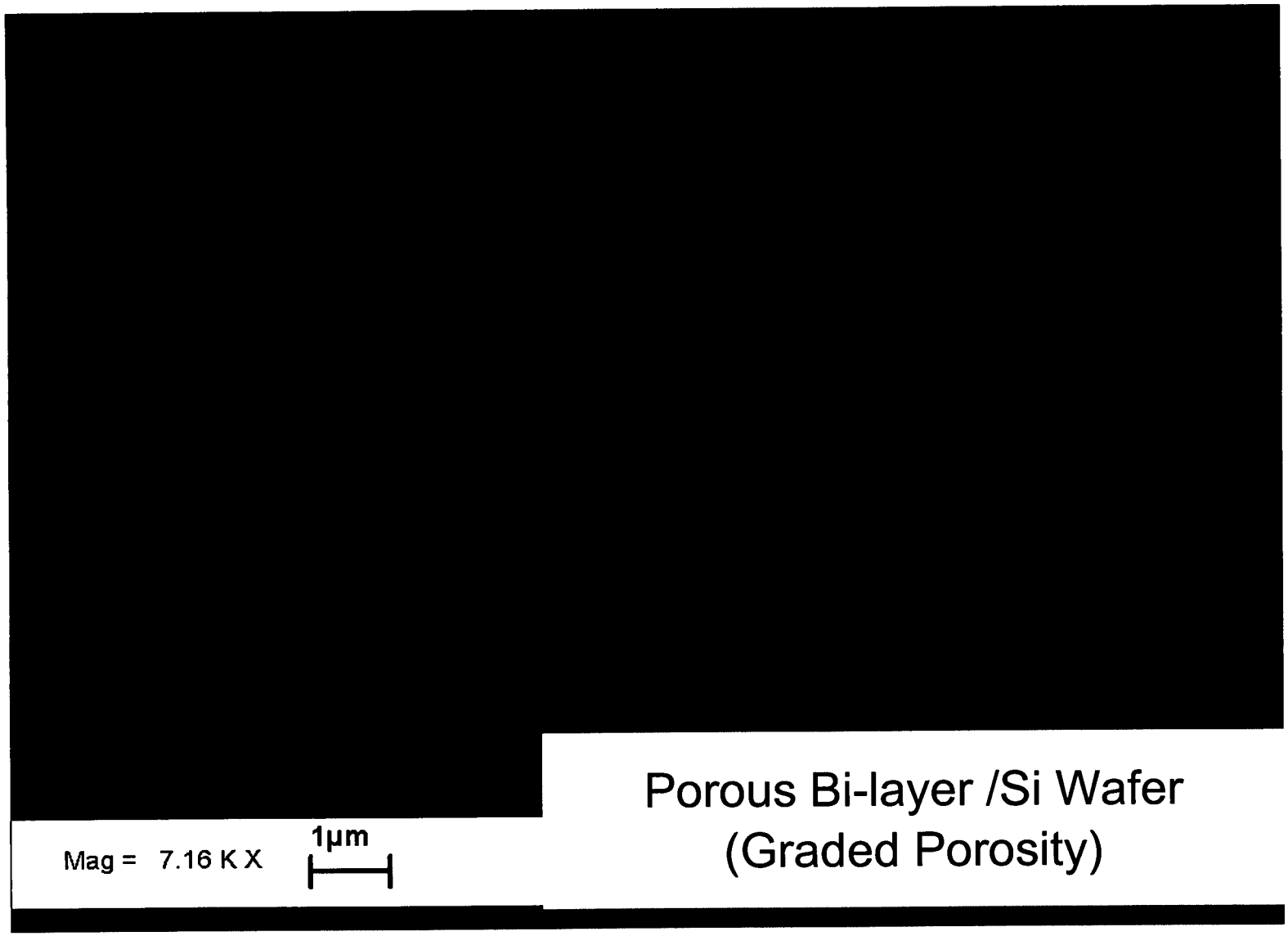
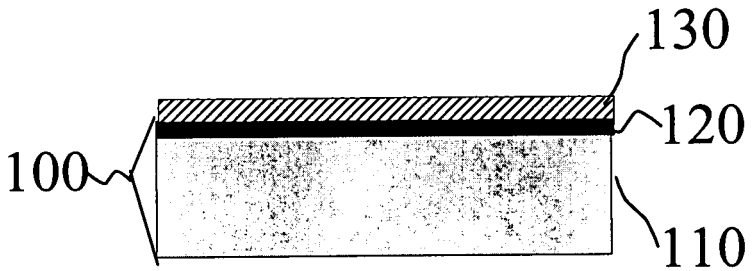
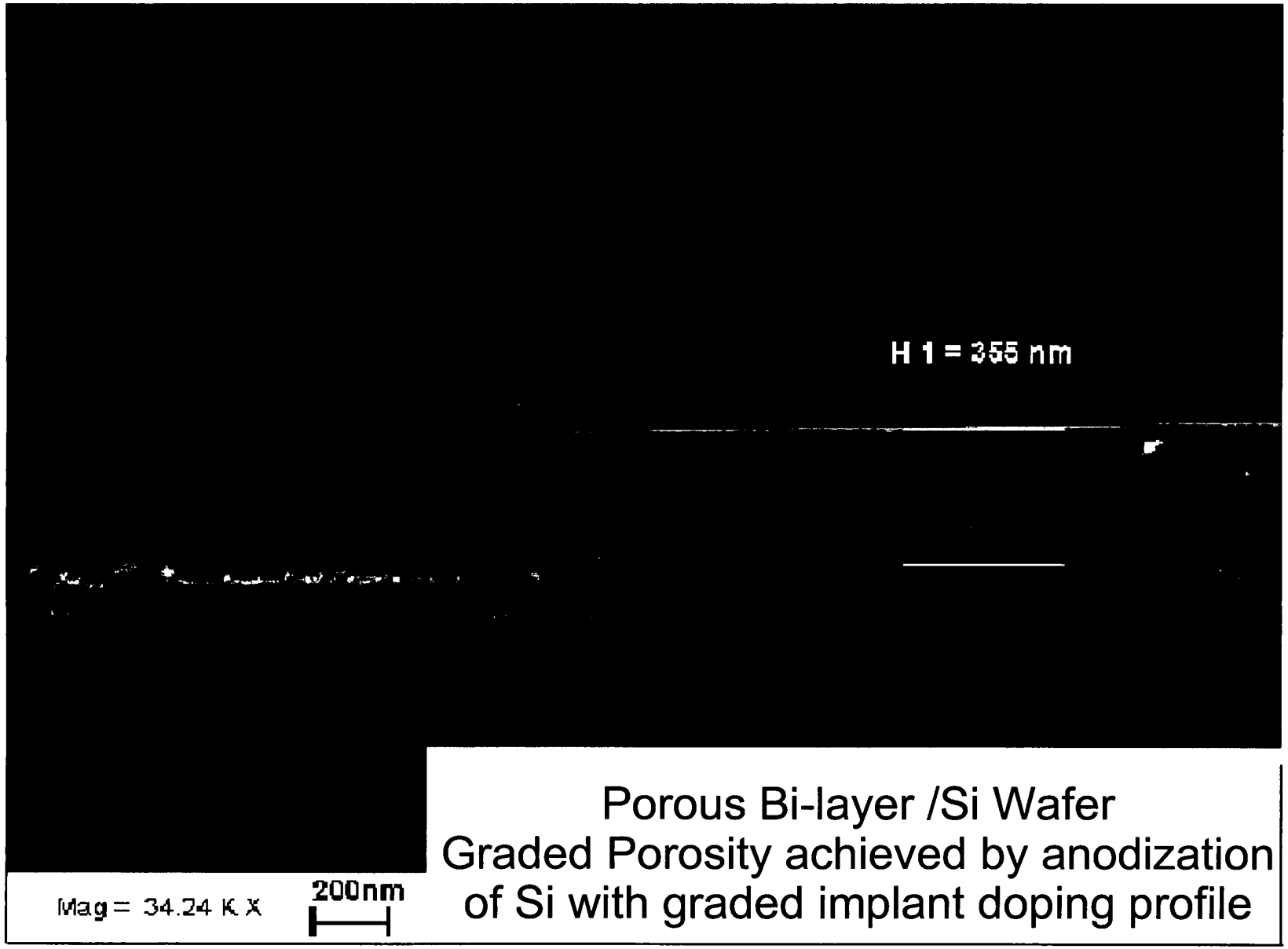


Figure 2



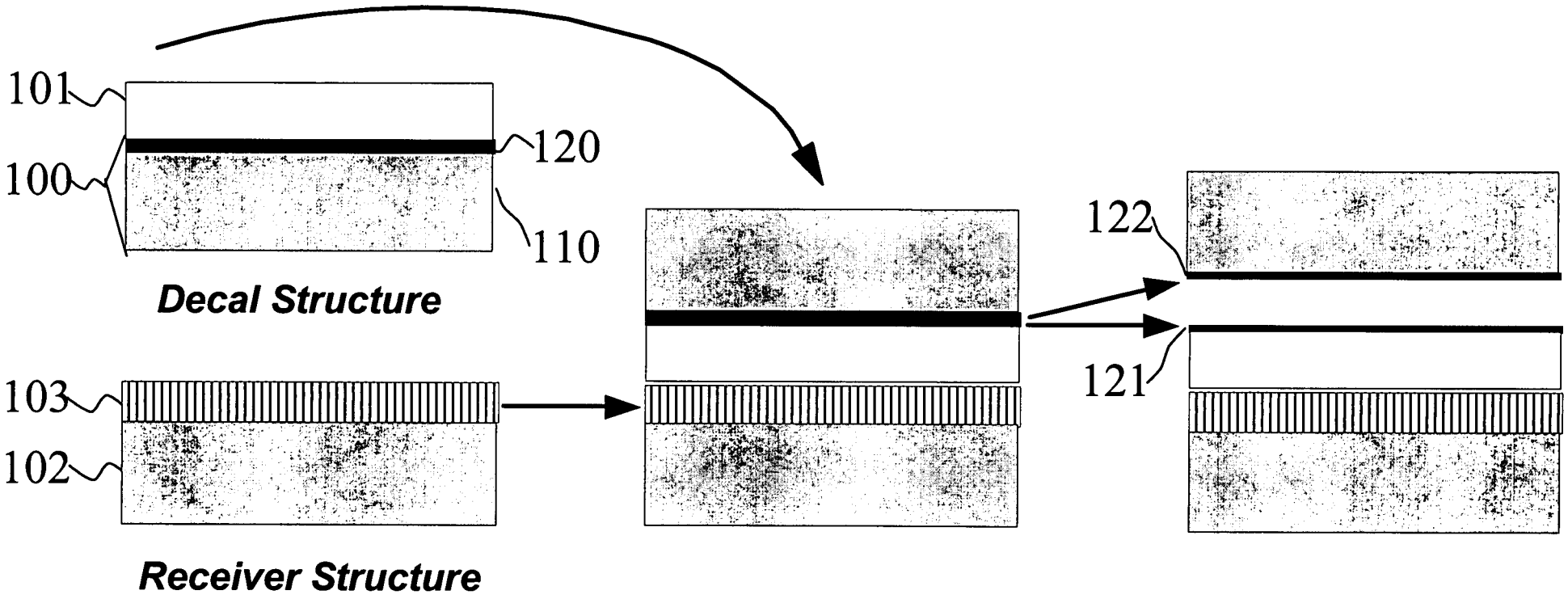
substrate based on use of the porous-Si layer
and subsequent regrowth of epi-Si layer to create SOI wafers

Figure 3



Porous Bi-layer /Si Wafer
Graded Porosity achieved by anodization of Si with graded implant doping profile

Figure 4

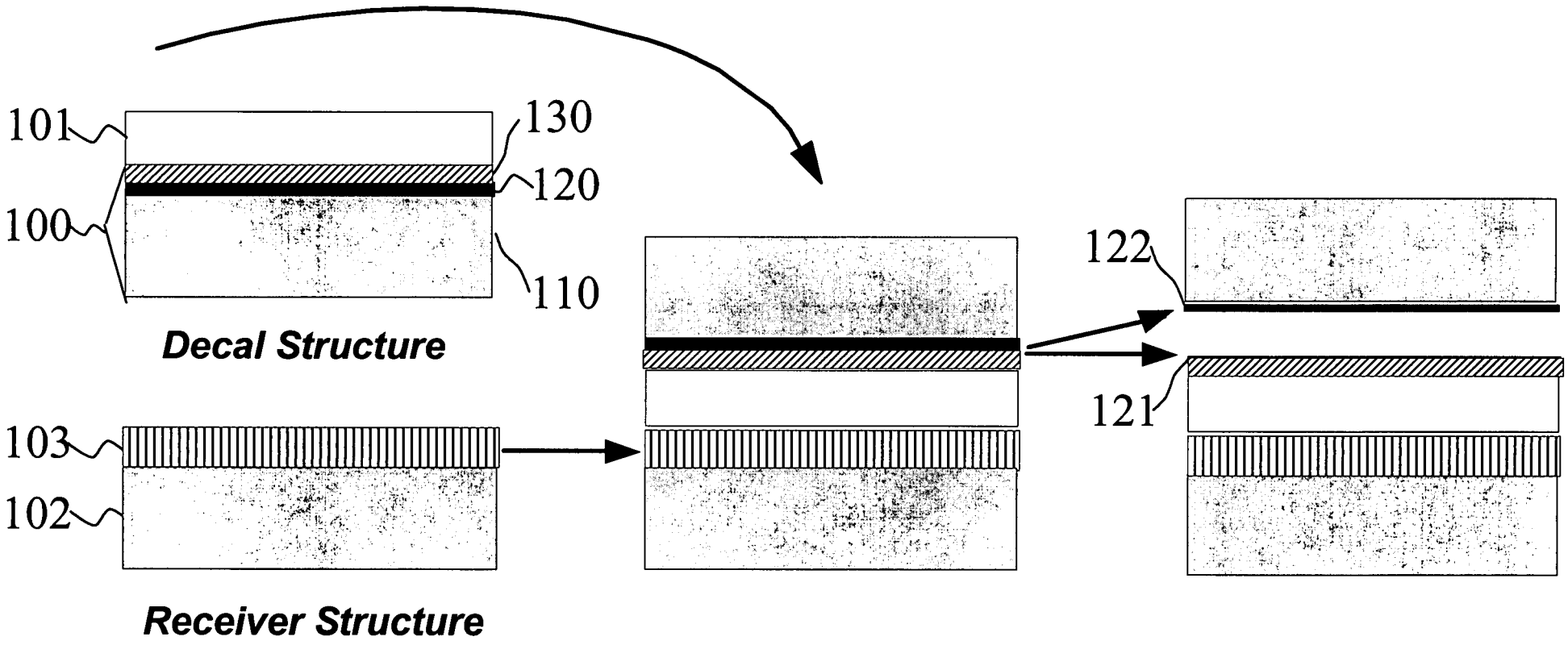


#1 Step: Build of Decal & Receiver Structures

#2 Step: Mating of Decal & Receiver Structures

#3 Step: Release of Carrier Substrate via Pealing

Figure 5



#1 Step: Build of Decal & Receiver Structures

#2 Step: Mating of Decal & Receiver Structures

#3 Step: Release of Carrier Substrate via Peeling